WHAT IS CLAIMED IS

1. A CMOS circuit including a pull-up transistor and a pull-down transistor, comprising:

(a) a first feedback circuit having an input coupled to a gate of the pull-up transistor and an output coupled to a gate of the pull-down transistor;

(b) a second feedback circuit having an input coupled to the gate of the pull-down transistor and an output coupled to the gate of the pull-up transistor;

(c) the first feedback circuit producing a first delayed signal on the gate of the pull-down transistor to turn on the pull-down transistor a first predetermined amount of time after the pull-up transistor is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor and the pull-down transistor; and

(d) the second feedback circuit producing a second delayed signal on the gate of the pull-up transistor to turn on the pull-up transistor a second predetermined amount of time after the pull-down transistor is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor and the pull-down transistor.

2. The CMOS circuit of claim 1 were in the pull-up transistor is a P-channel

transistor and the pull-down transistor is an N-channel transistor.

3. The CMOS circuit of claim 1 wherein the first and second feedback circuits each have an input for receiving an input signal.

4. A CMOS circuit including a P-channel pull-up transistor and an N-channel pull-down transistor, comprising:

(a) a P-channel first transistor having a source coupled to a first supply voltage and a gate coupled to a first input terminal for receiving a first input current, and an N-channel second transistor having a source coupled to a second supply voltage and a gate coupled to a second input terminal for receiving a second input current;

(b) a P-channel third transistor having a source coupled to the first supply voltage, a gate coupled to the first input terminal, and a drain coupled to a gate of the pull-up transistor, and an N-channel fourth transistor having a source coupled to the second supply voltage and a gate coupled to the second input terminal;

(c) a first feedback circuit having an input coupled to the gate of the pull-up transistor and an output coupled to a gate of a P-channel fifth transistor having a source coupled to a drain of the first transistor a drain coupled to a gate of the pull-down transistor and a drain of the second transistor, and a second feedback circuit having an input coupled to the gate of the pull-down transistor and an output coupled to a gate of an N-channel sixth transistor having a source coupled to a drain of the fourth transistor and a drain coupled to the gate of the pull-up transistor;

(d) the first feedback circuit producing a first delayed signal on the gate of the fifth transistor which causes the fifth transistor to turn on the pull-down transistor a first predetermined amount of time after the pull-up transistor is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor and the pull-down transistor, the second feedback circuit producing a second delayed signal on the gate of the sixth transistor which causes the sixth transistor to turn on the pull-up transistor a second predetermined amount of time after the pull-down transistor is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor and the pull-down transistor.

5. The CMOS circuit of claim 4 including a class AB control circuit coupled between the first and second input terminals.

6. The CMOS circuit of claim 4 wherein the first feedback circuit includes a first CMOS inverter, a first current source coupled between the first CMOS inverter and the second supply voltage, an input coupled to the gate of the pull-up transistor, and an output coupled to the gate of the fifth transistor.

7. The CMOS circuit of claim 4 wherein the fifth transistor is included in the first feedback circuit.

8. The CMOS circuit of claim 6 wherein the first CMOS inverter includes a P-channel seventh transistor having a source coupled to the first supply voltage and an N-channel eighth transistor having a drain coupled to the drain of the seventh transistor and a source coupled to the first current source.

9. The CMOS circuit of claim 6 wherein the second feedback circuit includes a second CMOS inverter, the second current source coupled between the second CMOS inverter and the first supply voltage, an input coupled to the gate of the pull-down transistor, and an output coupled to the gate of the sixth transistor.

10. The CMOS circuit of claim 9 wherein the sixth transistor is included in the second feedback circuit.

11. The CMOS circuit of claim 9 wherein the second CMOS inverter includes an N-channel ninth transistor having a source coupled to the second supply voltage and a P-channel tenth transistor having a drain coupled to the drain of the ninth transistor and a source coupled to the second current source.

12. The CMOS circuit of claim 4 wherein the first and second input currents are produced by a folded cascode stage of an input stage of a CMOS comparator circuit

13. The CMOS circuit of claim 12 including a class AB control circuit coupled between the first and second input terminals.

14. The CMOS circuit of claim 12 wherein the input stage of the CMOS comparator circuit is a differential input stage, and wherein the folded cascode stage is a differential folded cascode stage of the differential input stage of the CMOS comparator circuit.

15. A method of preventing shoot-through current in a CMOS circuit including a pull-up transistor and a pull-down transistor, the method comprising:

(a) providing a first feedback circuit having an input coupled to a gate of the pull-up transistor and an output coupled to a gate of the pull-down transistor, and a second feedback circuit having an input coupled to the gate of the pull-down transistor and an output coupled to the gate of the pull-up transistor;

(b) producing a first delayed signal on the gate of the pull-down transistor in response to a first signal on the gate of the pull-up transistor by means of the first feedback circuit to turn on the pull-down transistor a first predetermined amount of time after the pull-up

transistor is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor and the pull-down transistor; and

(c) producing a second delayed signal on the gate of the pull-up transistor in response to a second signal on the gate of the pull-down transistor by means of the second feedback circuit to turn on the pull-up transistor a second predetermined amount of time after the pull-down transistor is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor and the pull-down transistor.

16. The method of claim 15 wherein step (b) includes producing the first signal on the gate of the pull-up transistor in response to a transition of an input signal to a first level.

17. The method of claim 16 wherein step (c) includes producing the second signal on the gate of the pull-down transistor in response to a transition of the input signal to a second level.

18. A method of preventing shoot-through current in a CMOS circuit including a P-channel pull-up transistor and an N-channel pull-down transistor, the method comprising:

(a) applying a first input current to a gate of a P-channel first transistor having a source coupled to a first supply voltage and to a gate of a P-channel third transistor having a source coupled to the first supply voltage and a drain coupled to a gate of the pull-up transistor, and applying a second input current to a gate of an N-channel second transistor having a source coupled to a second supply voltage and a gate of an N-channel fourth transistor having a source coupled to the second supply voltage;

(b) producing a first delayed signal on a gate of a fifth transistor by means of a first feedback circuit having an input coupled to the gate of the pull-up transistor, a source coupled to a drain of the first transistor and a drain coupled to a gate of the pull-down transistor and a drain of the second transistor, and an output coupled to a gate of the fifth transistor to cause the fifth transistor to turn on the pull-down transistor a first predetermined amount of time after the pull-up transistor is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor and the pull-down transistor; and

(c) producing a second delayed signal on a gate of a sixth transistor by means of a second feedback circuit having an input coupled to the gate of the pull-down transistor, a source coupled to a drain of the fourth transistor and a drain coupled to the gate of the pull-up

transistor, and an output coupled to the gate of the sixth transistor to cause the sixth transistor to turn on the pull-up transistor a second predetermined amount of time after the pull-down transistor is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor and the pull-down transistor.

19. A CMOS circuit including a P-channel pull-up transistor and an N-channel pull-down transistor, comprising:

(a) a P-channel first transistor having a source coupled to a first supply voltage and a gate coupled to an input terminal for receiving an input voltage, and an N-channel second transistor having a source coupled to a second supply voltage and a gate coupled to the input terminal;

(b) a P-channel third transistor having a source coupled to the first supply voltage, a gate coupled to the input terminal, and a drain coupled to a gate of the pull-up transistor, and an N-channel fourth transistor having a source coupled to the second supply voltage and a gate coupled to the input terminal;

(c) a first feedback circuit having an input coupled to the gate of the pull-up

transistor and an output coupled to a gate of a P-channel fifth transistor having a source coupled to a drain of the first transistor and a drain coupled to a gate of the pull-down transistor and a drain of the second transistor, and a second feedback circuit having an input coupled to the gate of the pull-down transistor and an output coupled to a gate of an N-channel sixth transistor having a source coupled to a drain of the fourth transistor and a drain coupled to the gate of the pull-up transistor;

(d) the first feedback circuit producing a first delayed signal on the gate of the fifth transistor which causes the fifth transistor to turn on the pull-down transistor a first predetermined amount of time after the pull-up transistor is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor and the pull-down transistor, the second feedback circuit producing a second delayed signal on the gate of the sixth transistor which causes the sixth transistor to turn on the pull-up transistor a second predetermined amount of time after the pull-down transistor is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor and the pull-down transistor.

20. A CMOS comparator circuit comprising:

(a) a differential input stage including

i. a first input transistor having a gate coupled to receive a first input voltage signal, a source coupled to a tail current source, and a drain coupled to a junction between a source of a first cascode transistor and a drain of a first load transistor,

ii. a second input transistor having a gate coupled to receive the a second input voltage signal, a source coupled to the tail current source, and a drain coupled to a junction between a source of a second cascode transistor and a drain of a second load transistor,

iii. a bias source coupled to gates of the first and second cascode transistors, and circuitry for biasing gates of the first and second load transistors;

(b) a CMOS output stage including

i. a P-channel pull-up transistor and an N-channel pull-down transistor,

ii. a P-channel first transistor having a source coupled to a first supply voltage and a gate coupled to a first input terminal for receiving a first input current, and an N-channel second transistor having a source coupled to a second supply voltage and a gate coupled to a second input terminal for receiving a second input current,

iii. a P-channel third transistor having a source coupled to the first supply voltage, a gate coupled to the first input terminal, and a drain coupled to a gate of the pull-up transistor, and an N-channel fourth transistor having a source coupled to the second supply voltage and a gate coupled to the second input terminal,

iv. a first feedback circuit having an input coupled to the gate of the pull-up transistor and an output coupled to a gate of a P-channel fifth transistor having a source coupled to a drain of the first transistor and a drain coupled to a gate of the pull-down transistor and a drain of the second transistor, and a second feedback circuit having an input coupled to the gate of the pull-down transistor and an output coupled to a gate of an N-channel sixth transistor having a source coupled to a drain of the fourth transistor and a drain coupled to the gate of the pull-up transistor,

v. the first feedback circuit producing a first delayed signal on the gate of the fifth transistor which causes the fifth transistor to turn on the pull-down transistor a first predetermined amount of time after the pull-up transistor is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor and the pull-down transistor, the second feedback circuit producing a second delayed signal on the gate of the sixth transistor which causes the sixth transistor to turn on the pull-up transistor a second predetermined amount of time after the pull-down transistor is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor and the pull-down transistor; and

(c) circuitry for coupling a drain of the second cascode transistor to the first and second input terminals to supply the first and second input currents such that they represent the difference between the first and second input voltage signals.

21. The CMOS comparator circuit of claim 20 including a class AB control circuit coupled between the first and second input terminals.

22. A CMOS comparator circuit comprising:

(a) a differential input stage including

i. a first input transistor having a gate coupled to receive a first input voltage signal, a source coupled to a tail current source and a drain coupled to a drain of a first load transistor,

ii. a second input transistor having a gate coupled to receive the a

second input voltage signal, a source coupled to the tail current source and a drain coupled to a drain of a second load transistor,

iii. a bias source coupled to gates of the first and second cascode transistors, and circuitry for biasing gates of the first and second load transistors;

(b) a CMOS output stage including

i. a P-channel pull-up transistor and an N-channel pull-down transistor,

ii. a first feedback circuit having a first input coupled to the drain of one of the first and second input transistors and a second input coupled to a gate of the pull-up transistor, and an output coupled to a gate of the pull-down transistor,

iii. a second feedback circuit having a first input coupled to the drain of one of the first and second input transistors and a second input coupled to the gate of the pull-down transistor, and an output coupled to the gate of the pull-up transistor,

iv. the first feedback circuit producing a first delayed signal on the gate of the pull-down transistor to turn on the pull-down transistor a first predetermined amount of time after the pull-up transistor is turned completely off so as to prevent any shoot-through

current from flowing through the pull-up transistor and the pull-down transistor, and

v. the second feedback circuit producing a second delayed signal on the gate of the pull-up transistor to turn on the pull-up transistor a second predetermined amount of time after the pull-down transistor is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor and the pull-down transistor.

23. The CMOS output stage of claim 22 wherein the first input of the first feedback circuit is coupled to the drain of one of the first and second input transistors by means of a first cascode transistor.

24. The CMOS output stage of claim 23 wherein the first input of the second feedback circuit is coupled to the drain of the other of the first and second input transistors by means of a second cascode transistor.